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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,655	09/25/2003	Yasushi Kinoshita	Q77597	5578
23373	7590	08/27/2004	EXAMINER	
SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVENUE, N.W. SUITE 800 WASHINGTON, DC 20037			GEBREMARIAM, SAMUEL A	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 08/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/669,655

Applicant(s)

KINOSHITA, YASUSHI

Examiner

Samuel A Gebremariam

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

**DETAILED ACTION**

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 1 and 2 are rejected under 35 U.S.C. 102(e) as being anticipated by Belleville et al., US Pub. No. 2002/0094629 A1.

Regarding claim 1, Belleville teaches (fig. 8) a semiconductor integrated circuit comprising a power supply wiring (418 and 420, also refer to paragraph 0079 and 0080) and a ground wiring (layer 110 combined with the substrate provides grounding) and a decoupling capacitor (110, 112, 114, refer to the abstract) formed between the power supply wiring and the ground wiring, wherein at least one of the electrodes (110) of the decoupling capacitor consists of a shield layer formed in a plane shape on a semiconductor substrate (102), and the shield layer is connected electrically directly to the semiconductor substrate and is fixed to a power supply potential or the ground potential (paragraph 0083).

Regarding claim 2, Belleville teaches (fig. 8) substantially the entire claimed structure of claim 1 above including out of the electrodes of the decoupling capacitor, the electrode (114) opposing the electrode consisting of the shield layer (110) consists of a wiring layer (the plugs making contact to 420) connected to wirings on the

uppermost layer of a multi-layer wiring structure via contact electrodes, and a capacitor insulating film (112) for forming the decoupling capacitor is provided between the wiring layer and the shield layer (110).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Belleville in view of Emma et al. US patent No. 6,285,050.

Regarding claim 3, Belleville teaches (fig. 8) substantially the entire claimed structure of claim 1 above except explicitly stating that the shield layer is obtained by covering a plurality of protrusions formed on the substrate.

It is conventional in the art and also taught by Emma forming capacitor electrodes (M3) on protruded structure (fig. 2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Emma of forming a thin film decoupling capacitor in the structure of Belleville in order to form a reliable decoupling capacitor.

Regarding claim 4, Belleville teaches (fig. 8) substantially the entire claimed structure of claims 1 and 3 above including a gate electrode.

The limitation that the protrusions are formed simultaneously with the gate electrode by the identical formation process for the gate electrode is not given patentable weight because, this is considered a product-by-process claim. “[E]ven though product-by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.” *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Regarding claim 5, Belleville teaches (fig. 8) substantially the entire claimed structure of claims 1 and 3 including the decoupling capacitor is formed on element isolation oxide film.

Since the combined structure of Belleville and Emma teaches an integrated circuit with CMOS and MIM structure, the combined structure would have an element isolation region.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Belleville, Emma and in view of Kinseki JP patent No. 08037281A.

Belleville teaches (fig. 8) substantially the entire claimed structure of claims 1 and 3 except explicitly stating that the shield layer consists of a silicon compound of a metal.

Kinseki teaches the use of silicide film as a capacitor electrode in the structure of forming a bypass capacitor.

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It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the silicide capacitor electrode taught by Kinseki in the structure of Belleville in order to increase the conductivity of the electrode.

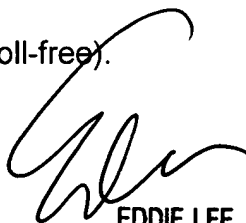
***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG  
August 20, 2004

  
EDDIE LEE  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800